AMENDMENTS TO THE SPECIFICATION AND ABSTRACT

Please amend the paragraph beginning on page 2, line 21 as follows:

The operation of the video composition circuit constructed as described above will be described with reference to figure ~~4~~ 5.

Please amend the paragraph beginning on page 3, line 1 as follows:

During a main video 1 transfer period ~~403~~ 503, main video data ~~408~~ 508 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and stored as main video 1 (~~411~~511) in the internal storage unit 303. Subsequently, during a main video 2 transfer period ~~404~~ 504, another main video data ~~408~~ 508 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the main video data ~~408~~ 508 is transferred to the main video output unit 306 and processed, and stored as data ~~412~~ 512 after main video filtering in the internal storage circuit 303.

Please amend the paragraph beginning on page 3, line 12 as follows:

Next, during a sub video transfer period ~~405~~ 505, sub video data ~~409~~ 509 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the sub video data ~~409~~ 509 is transferred to the sub video output unit 305 and processed, and the processed main video and sub video data ~~413~~ 513 is stored in the internal storage circuit 303.

Please amend the paragraph beginning on page 3, line 18 as follows:

Next, during an OSD transfer period ~~406~~ 506, OSD display data ~~410~~ 510 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the OSD display data ~~410~~ 510 is transferred to the OSD output unit 304 and processed. Furthermore, in the subsequent-stage video output unit 307, the OSD display data processed by the OSD output unit 304 and the previously processed main video and sub video data ~~413~~ 513 are combined, thereby obtaining final output data ~~414~~ 514.

Please amend the paragraph beginning on page 4, line 2 as follows:

In the operation of the above-mentioned circuit, the processings are finally carried out in synchronization with a display period ~~402~~ 502 which is a display speed of frames based on a horizontal sync signal ~~401~~ 501.

Please amend the paragraph beginning on page 5, line 2 as follows:

In order to solve the above-mentioned problems, according to Claim 1 of the present invention, there is provided a video composition circuit for receiving plural pieces of video data which are successively inputted in serial order, performing a predetermined video processing for predetermined video data, and combining plural pieces of video data to output composite data, and the video composition circuit comprises: a video processing unit to which plural pieces of video data are successively inputted in serial order, performing a predetermined video processing to the inputted video data, and outputting the processed video data; a video data composition unit for combining the plural pieces of video data outputted from the video processing ~~circuit~~ unit to output composite data; and a data storage unit for holding the video data outputted from the video data composition unit; and the video data composition unit being a circuit having an α - blending function, and combining the video data read from the data storage unit and the video data outputted from the video processing unit, as well as combining the plural pieces of video data outputted ~~read~~ from the video processing unit, thereby performing vertical filtering to the video data successively inputted in serial order and to the α – blended video data stored in the data storage unit ~~and the video data outputted from the video processing circuit, as well as combining the plural pieces of video data outputted from the video processing circuit~~.

Please amend the paragraph beginning on page 5, line 25 as follows:

According to Claim 3 of the present invention, in the video composition circuit defined in Claim 1, the plural pieces of video data successively inputted in serial order are main video, sub video, and OSD video which is additional information to be

displayed simultaneously with the main and sub videos~~; and the video data composition unit is a circuit having an α-blending function~~.

Please amend the paragraph beginning on page 6, line 16 as follows:

~~According to Claim 5 of the present invention, in the video composition circuit defined in Claim 3, the video data composition unit having the α-blending function reads the video data outputted from the external storage unit, and the α-blended video data which is stored in the data storage unit in the chip, and subjects these data to vertical filtering.~~

Please amend the paragraph beginning on page 7, line 4 as follows:

As described above, according to Claim 1 of the present invention, there is provided a video composition circuit for receiving plural pieces of video data which are successively inputted in serial order, performing a predetermined video processing for predetermined video data, and combining plural pieces of video data to output composite data, and the video composition circuit comprises: a video processing unit to which plural pieces of video data are successively inputted in serial order, performing a predetermined video processing to the inputted video data, and outputting the processed video data; a video data composition unit for combining the plural pieces of video data outputted from the video processing unit ~~circuit~~ to output composite data; and a data storage unit for holding the video data outputted from the video data composition unit; and the video data composition unit being a circuit having an α - blending function, and combining the video data read from the data storage unit and the video data outputted from the video processing ~~circuit~~ unit, as well as combining the plural pieces of video data outputted from the video processing ~~circuit~~ unit, thereby performing vertical filtering to the video data successively inputted in serial order and to the α - blended video data stored in the data storage unit. Therefore, the circuit scale can be reduced by integrating the video processing unit, the video data composition unit, and the data storage unit on a single circuit.

Please amend the paragraph beginning on page 8, line 5 as follows:

According to Claim 3 of the present invention, in the video composition circuit defined in Claim 1, the plural pieces of video data successively inputted in serial order are main video, sub video, and OSD video which is additional information to be displayed simultaneously with the main and sub videos~~; and the video data composition unit is a circuit having an α-blending function~~. Therefore, there is required only one α-blending circuit having an OSD display function, a sub video display function, a main video display function, and an α-blending function, whereby the circuit scale can be reduced. Further, since the OSD output unit, the sub video output unit, and the main video output unit are united to be one circuit, functions which have conventionally been realized for sub video but have not been realized for OSD can be used for OSD.

Please amend the paragraph beginning on page 9, line 5 as follows:

~~According to Claim 5 of the present invention, in the video composition circuit defined in Claim 3, the video data composition unit having the α-blending function reads the video data outputted from the external storage unit, and the α-blended video data which is stored in the data storage unit in the chip, and subjects these data to vertical filtering. Therefore, the internal storage unit is used so that data are overwritten, whereby the amount of usage of the internal storage unit can be reduced.~~